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Schroeder, D.; Hines, R.;

Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [see also IEEE Trans. on Components, Packaging, and Manufacturing Technology, Part A, B, C], Volume: 3 Issue: 3, Sep 1980

Page(s): 367 -369

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2 The effect of copper contamination on field overlap edges and perimeter junction leakage current

Vermeire, B.; Lee, L.; Parks, H.G.;

Semiconductor Manufacturing, IEEE Transactions on, Volume: 11 Issue: 2, May 1998

Page(s): 232 -238

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3 Defect-oriented Verilog fault simulation of SoC macros using a stratified fault sampling technique

Santos, M.B.; Goncalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;

VLSI Test Symposium, 1999. Proceedings. 17th IEEE, 25-29 April 1999

Page(s): 326 -332

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4 Defect-oriented mixed-level fault simulation of digital systems-on-a-chip using HDL

Santos, M.B.; Teixeira, J.P.;

Design, Automation and Test in Europe Conference and Exhibition 1999.

Proceedings , 9-12 March 1999
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... more thoroughly using auto-report and **zoom**-in analysis ... Confidential Yield, Performance, Profitability **Layout** Attribute Extractions ... 2 4 6 8 10 12 **Defect** size (um ...

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... image, independent of feature size, with the ability to **zoom** in an ... abstract representations with no relationship to the physical **layout** to **defect** models or ...

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... screen parameters, inspect pattern against circuit **layout**. ... inspection criteria descriptions and **defect** codes. ... Used--Nikon Stereoscopic **Zoom**, Unitron Measuring ...

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... below 10 W/cm²). However, CMOL technology imposes substantial restrictions (most impor- tantly, that of high **defect** tolerance) on ... (b) A **zoom**-in showing ... rsfq1.physics.sunysb.edu/~likharev/nano/Springer04.pdf - [Similar pages](#)

S/390 G5 CMOS microprocessor diagnostics

... A standard infrared microscope is used to **magnify** and focus ... The **defect** is modeled by a series resistor in the B ... the B clock signal to the p-FET device **layout**.

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... On-chip **integrated circuit** speed selection, 5,099,196, ... Trace conductor **layout**

configuration for preserving signal ... Method and controller for **defect** tracking in ...
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... to less than 0.1°C, **zoom**, live image ... on an IC using wafer **defect** inspection data. ... Demo #19: **INTEGRATED CIRCUIT RELIABILITY TESTING** —Micro Instrument Co ...
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... above do not include the design, **layout** or logistics ... OR THAT THE SOFTWARE IS WITHOUT **DEFECT** OR ERROR ... Plus, Zip Rescue and design, Zip Unleashed!, and Zip **Zoom**. ...
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donde linux

... It works in conjunction with external **layout** tools, including VCG ... rtp also allows the user to **zoom** in and ... of the program is to simulate **defect** structures and ...
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5218717 Simulcast transmission system with improved synchronizing ...

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... Figure 4-1: Controller **Layout**. ... **Zoom** - The AquaRAD SL uses the **zoom** switch to operate the ... with reasonable opportunity to verify the alleged **defect** by inspection

...
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... simulation is added right after the IC **layout** design ... of failures at **defect** site
Sample group S M S M S M ... reliability because it makes possible to **zoom** into the

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... 27 **Zoom** A pulse might represent one bit of information traveling through a computer circuit or it might be a glitch, or **defect**, in a circuit. ...

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... It is then easy and applicable for employing it into **Integrated Circuit** (IC) realization to ... This paper presents a CMOS circuit suitable to **magnify** the value of ...

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... **Defect** Sample Planning, if part of a planning process and **layout** for 300 mm fabs,
can help manufacturers achieve the gains they seek as they move to the new ...
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... The Canadian microelectronics and **integrated circuit** (IC) packaging and
electronic components industries combined for an output of about \$4.3 billion in 1996.
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... An application specific **integrated circuit** (ASIC) has been designed to control four
of the 24 phases in a stator unit. This **integrated** ...
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... may facilitate rapid scanning of slides containing cell specimen, reduce several
human operator hours and thus minimise human errors, pan and **zoom** on specific ...
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... list which factors in the technology, **layout**, and process ... but not sufficient
condition to achieve high **defect** coverage ... of abstraction in order to **zoom** into the
...
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... cards' micro-structural 'signature', by probing at the nano-**defect** level ... Failure

analysis could also extend within the **integrated circuit** itself, allowing ...
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[DOC] NAVY

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... signature', by probing at the nano-**defect** level. ... could also extend within the **integrated circuit** itself, allowing ... T/R) modules and proposing a **layout** of the ...
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... \$300 billion per year for global **integrated circuit** sales (R ... reveals how competitive the effort to **magnify** the economic ... was given to the interior **layout** of the ...
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EP1229481

... portions 172 or 174 develop a **defect**, each row is ... Xia functionality, such as pan, **zoom** and pixel ... temperature monitoring, unique board ID, **layout** revision number ...
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HARDWARE SETUP 14 3.1 Motherboard **Layout**
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... shall not apply to any **defect**, failure or ... Information 2-7 Screen **Layout** 2-7

...

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... Page 10. TM0010 Page 10 of 86 Issue 2.01 View Graphics (Overview - page 1 of 4) View Graphics (**zoom** level – page 2 of 4) Page 11. ...

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... a H1 (one missing hole) cavity, much studied as, eg, a lasing **defect** on a ... guided mode, giving rise to the transmission MSB [see the **zoom** in Fig ... a) **Layout** of the ... imowww.epfl.ch/GMS/Houdre/Articles/JQE_Cascaded.pdf - Supplemental Result -

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... any program that allows pixel-by-pixel modification through a **zoom** feature ... n. A physical **defect**, such as a loose connection, that prevents a system ... file **layout**. ...

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... OF SUCH DAMAGES ARISING FROM ANY **DEFECT** OR ERROR ... V2740 Series **Layout** I. Introduction I. Introduction **Layout** Video-In ... box to move your screen or to **zoom** in and ...

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... such damages arising from any **defect** or error ... components contain very delicate **Integrated Circuit** (IC) chips ... illustration below shows the **layout** and connectors ...

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... Arrays of vertical rods are mounted in base plates; baseplate pattern **layout** will be different for the various crystal structures. ...

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HARDWARE SETUP 16 **Layout** Contents 3 ... and expansion cards contain delicate

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... Placement of holes in the base-plate **layout** and the location of spacers are ...
After mounting in a tensile-testing apparatus, a stereo-**zoom** microscope is mounted

...
wiley.com/college/msci/callister39551X/demonstrations/demonstrations.pdf -

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... BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES ARISING FROM
ANY **DEFECT** OR ERROR ... 10 ASUS AGP-V3800 Ultra Series **Layout**

gtruhanov.iki.rssi.ru/ftp/drivers/ASUS/V3800.AGP/v3800-104.pdf - Supplemental

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Patent 4779210: Graphic processing apparatus

... of 2. This method is accompanied by a **defect** that it ... Next, the bit **layout** of the
respective data to be ... This embodiment is constructed of a **zoom** X control unit ...

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... For exam-ple, in XP, small working software releases are released regularly and if
the released software contains a **defect**, it is easier to trace the items ...

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... OF SUCH DAMAGES ARISING FROM ANY **DEFECT** OR ERROR ... Reset Switch
Lead (2 pin) **Layout** Contents3. ... expansion cards contain very delicate **Integrated
Circuit (IC) chips** ...

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[PDF] NO. 356 May 1999 Japanese Companies in the United States American ...

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... includes built-in speakers and a laser pointer as well as manual **zoom** and wireless
... wafers that also is dual capable; (4) an optical shallow **defect** analyzer for ...

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AKAI FAQ PAGE

... The ZIP **zoom** scsi card is actually an Adaptec 1502 ... a not completely standard
connector pin **layout** so get ... your floppies are formatted and 100% **defect** free, try

...
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... array research should focus on on-chip processing, **layout**, mounting, and ...
specific integrated circuits (ASIC), and ultra large **integrated circuit** (ULSIC) chips ...
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... and the address of the manufacturer included on the cabinet **layout** and master ...
Pin 1 for all **integrated circuit** packages shall be designated on all printed ...
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... OF SUCH DAMAGES ARISING FROM ANY **DEFECT OR ERROR** ... Management
Interrupt Lead (2 pin) **Layout** Contents 3 ... cards contain very delicate **Integrated Circuit** (IC) chips. ...
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... of new technologies--first the transistor, next the **integrated circuit**, and finally ...

1984, for example, the crafts of typography and page **layout** were practiced ...

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DVI **Layout** ... and components contain very delicate **Integrated Circuit** (IC) chips ...

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... of the possibility of such damages arising from any **defect** or error ... **Zoom**-in to any

part of the screen. ... s Manual 13 ASUS 3DP-V264GT2/TV **Layout** AMC Connector ...

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Pure **Layout**

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... to use the versatility of automated **zoom** lenses in ... sensor,employs a fully customized

integrated circuit implemented in a 2u. ... was to detect a surface **defect** in a ...

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... system you use (eg VHS, S-VHS, Hi8, Video 8). Audio devices Internal/external audio

output (optional): The internal audio output (see board **layout** below, ST 7 ...

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... 공구 1721 Crip 크립 1722 critical altitude 임계고도 1723 Critical Angle 임계각

1724 Critical Area 임계부 1725 critical **defect** 치명적 결함 ...

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... OF SUCH DAMAGES ARISING FROM ANY **DEFECT** OR ERROR ... instead of following the pin **layout**

on the ... as SCSI cards, contain very delicate **Integrated Circuit** (IC) chips. ...

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